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Optimizing PI Controller Performance in Ultra Step-Up Converters Using Particle Swarm Optimization

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Abstract

The development of electric vehicles (EVs) drives the need for high-voltage ratio DC-DC step-up converters capable of connecting low-voltage battery power sources to electric drive systems and auxiliary systems requiring high voltages. This study proposes a non-isolated ultra step-up converter incorporating a diode–capacitor–inductor (D–C–L) unit at the input and a voltage multiplier cell (VMC) at the output. This topology achieves high voltage gain at low duty cycles while reducing voltage stress on semiconductor devices, enabling the use of lower-rated components and improving overall efficiency. Two control strategies were evaluated: a conventional Proportional–Integral (PI) controller and a PI controller tuned using Particle Swarm Optimization (PSO). MATLAB/Simulink simulations show that the PSO-PI controller outperforms the conventional PI, reducing overshoot from 21.7% to 8.7%, settling time from 227.78 ms to 117.78 ms, and voltage deviation during load changes from ±35 V to ±15 V. Recovery time under disturbances was also shortened from 0.4 s to as low as 0.15 s. These results confirm that PSO-based tuning enhances voltage regulation, transient performance, and robustness, making it a promising solution for ultra step-up converters in EV applications powered by 48 V sources.

Keywords: Ultra step-up converter; optimization; particle swarm optimization-pi controller; dynamic response; stability.

1. Introduction

The rapid development of electric vehicles (EVs) has driven an increasing demand for high-voltage ratio DC-DC step-up converters, particularly to connect low-voltage battery sources (e.g., 12–48 V) to the high-voltage levels required by electric drive systems and auxiliary subsystems. These converters play a crucial role in ensuring efficient power conversion within modern EV architectures.

Conventional boost and buck–boost converters have been widely used due to their simplicity and cost-effectiveness. Theoretically, traditional boost DC-DC converters can achieve high output voltage at extreme duty cycles. However, in practice, the voltage stress across the main switch becomes equal to the high output voltage, posing a challenge. Several other DC-DC converter topologies, such as Quadratic Boost Converters, Cascaded Boost Converters, and Interleaved Boost Converters, also face performance limitations at high voltage gain, particularly at extreme duty cycles. The presence of parasitic elements like the equivalent series resistance (ESR) of inductors and capacitors, as well as non-ideal characteristics of semiconductors, significantly degrade efficiency and voltage boosting capability. Additionally, high voltage stress on the main switch complicates control mechanisms, increases the risk of component failure, and reduces overall system reliability [1], [2].

To address these challenges, advanced step-up converter designs have been proposed, incorporating features such as multi-stage architecture, coupled inductors, and voltage multiplier cells (VMCs). These configurations improve voltage gain while reducing stress on components, thereby enhancing efficiency. Among these innovations, integrating diode–capacitor–inductor (D–C–L) units at the input side and VMCs at the output has demonstrated promising results in achieving high voltage gain at lower duty cycles. This structure effectively reduces voltage stress on semiconductor devices, enabling the use of lower-rated components and enhancing system reliability [3].

In EV applications, the demand for high-voltage output to drive electric motors is critical, particularly when supplied by low-voltage batteries. Efficient power conversion not only maximizes battery utilization but also extends driving range and enhances vehicle performance. Ultra step-up converters are utilized to meet these needs due to their capability to significantly boost voltage with high efficiency. As transformerless DC-DC circuits, ultra step-up converters offer advantages in terms of simple design, compact size, and high efficiency compared to transformer-based converters. Therefore, the proposed ultra step-up converter design is expected to provide optimal performance for electric motor applications and serve as a reliable solution for EV systems [4], [5], [6].

Accordingly, this paper focuses on optimizing the performance of a PI controller in an ultra step-up DC–DC converter using the Particle Swarm Optimization (PSO) algorithm. The objective is to improve output voltage regulation and transient response under varying load conditions by tuning the controller gains using PSO. The key contributions of this study include: (1) the application of PSO to determine optimal PI parameters, and (2) a comparative performance analysis between conventional PI and PSO-PI controllers under disturbance scenarios, validated through detailed MATLAB/Simulink simulations.

2. Method

2.1. Overview of Ultra Step-Up Converter

The proposed DC–DC converter is designed to overcome the limitations of conventional boost converters, such as efficiency losses, high voltage stress, and control complexity at extreme duty cycles. By integrating multiple diode–capacitor–inductor (D–C–L) units on the input side and voltage multiplier cells (VMCs) on the output side, the converter achieves high voltage gain while maintaining low voltage stress on semiconductor components[3], [7].

A. Circuit Description

This converter employs a modular architecture combining n-stage D–C–L units and VMCs. Each D–C–L unit comprises a diode, a capacitor, and an inductor connected in a series configuration on the input side, contributing to the initial voltage boosting and energy storage. On the output side, VMCs further enhance the voltage gain without significantly increasing circuit complexity. The modular nature of this design ensures scalability for higher gain applications.[8] .

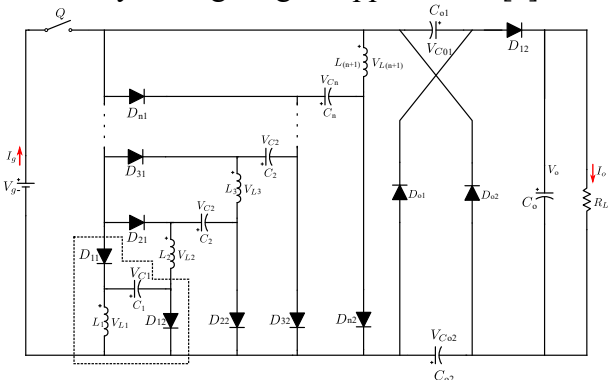

Figure 1. Generalised converter proposed

The overall structure of the proposed converter is illustrated in Figure 1. Key components and their functions include:

- **Input D–C–L Units**: Provide initial voltage boosting and energy buffering.
- **Switch Q**: Controls energy transfer between the input and output stages.
- **Output VMCs**: Further increase output voltage and stabilize the output.

B. Principle of Operation

The ultra step-up converter operates in three modes: Continuous Conduction Mode (CCM), Boundary Conduction Mode (BCM), and Discontinuous Conduction Mode (DCM).

1. Continuous Conduction Mode (CCM)

Continuous Conduction Mode refers to the condition where the current through the inductor never drops to zero during the entire switching cycle. There are two time intervals corresponding to the states of the switching component—when the switch is on (closed) and when it is off (open).

First Interval ($0 < t < dT_s$): During this interval, switch Q is turned on. The capacitors $C_1, C_2, \dots C_n$ and inductors $L_1, L_2, \dots, L_{n+1}$ are charged by the input power supply. Diodes D_{o1} and D_{o2} are reverse-biased, and the load receives power from the energy stored in the output capacitors C_{o1} and C_{o2}.

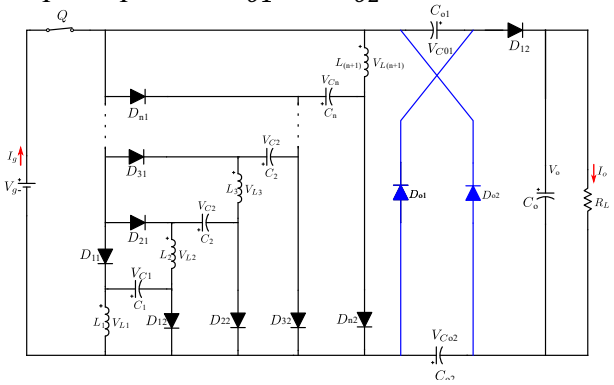

Figure 2. Equivalent circuit during the ON interval (T_{ON})

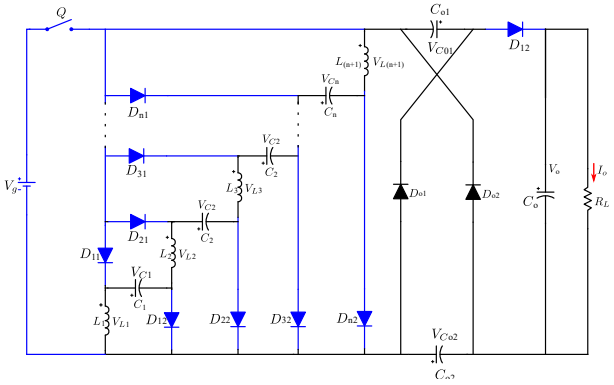

Figure 3. Equivalent circuit during the OFF interval (T_{OFF})

Second Interval ($dT_s < t < T_s$): Switch Q is turned off. The energy stored in the inductors and capacitors is transferred to the load through the voltage multiplier stage.

The equivalent circuit representations for both intervals are shown in Figure 2 and Figure 3, respectively, illustrating the operational changes during each switching state. The voltage gain (M) for the proposed converter in Continuous Conduction Mode (CCM) is derived based on the input and output parameters, as shown in (1).

$$M_{CCM} = \frac{V_o}{V_g} = \frac{I_g}{I_o} = \frac{2n + D + 1}{1 - D} \qquad (1)$$

Where:

- d is the duty cycle,
- n is the number of D–C–L units.

Increasing the number of D–C–L stages results in a higher voltage gain[1], [7].

2. Discontinuous Conduction Mode (DCM)

In this mode, the current through the inductor drops to zero for a certain period before the next switching cycle begins. During this time, the inductor does not store any energy. The equivalent circuit of the converter in DCM during the third time interval$[(d + d_2)T_S < t < T_S]$ is shown in Figure 4. Here d_2 represents the normalized duration starting from the moment when the inductor current begins to decrease $t_1 < t < t_2$ until it reaches zero. The current through inductor L_1 (i_{L1}) under DCM is illustrated in Figure 5. where it can be seen that the current drops to zero and remains there until switch Q is turned on again.

Sencond Interval ($dT_S < t < T_S$):

- Switch Q is turned off.
- Capacitors $C_1, C_2, \dots, C_n$ and inductors $L_1, L_2, \dots, L_{n+1}$ are connected in series, transferring energy to the output capacitors C_{o1} and C_{o2} via the voltage multiplier cell (VMC).

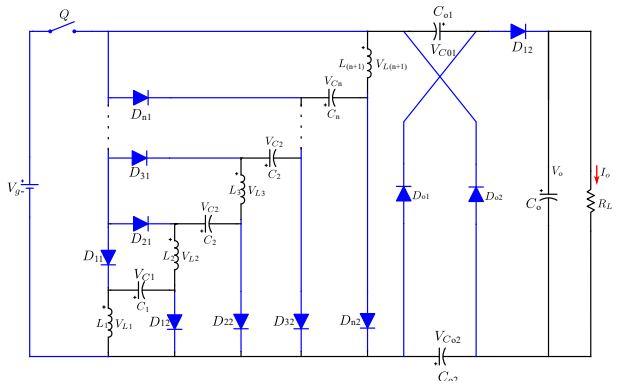

Figure 4. Equivalent circuit of the converter under DCM

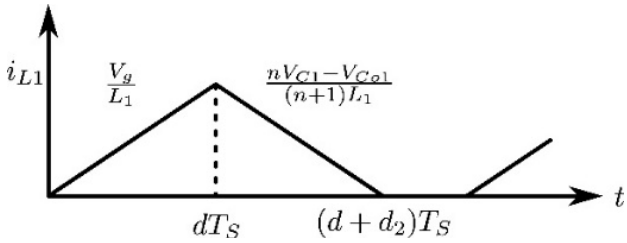

Figure 5. Inductor current $L_1(i_{L1})$ waveform under DCM

Knowing that the average voltage across inductor L1 over one switching cycle is zero, the normalized duration d_2 which represents the interval when the inductor current decreases to zero can be calculated using (2).

$$d_2 = \frac{2(n+1)DV_g}{V_o - (2n+1)V_g} \tag{2}$$

Given the value of d_2 and referring to Figure Figure 5, the inductor current reaches its peak value $(I_{L1,Peak})$ at $t = dT_S$. This peak current can be expressed analytically as shown in (3).

$$i_{L1}(t = DT_S) = I_{L1,Peak} = \frac{V_g}{L_1} dT_S \tag{3}$$

3. Boundary Conduction Mode (BCM)

In BCM, the inductor current falls to zero exactly at the end of each switching cycle. This indicates that the inductor completely discharges its energy just as the cycle ends and begins storing energy again at the start of the next cycle. BCM lies at the boundary between CCM and DCM.

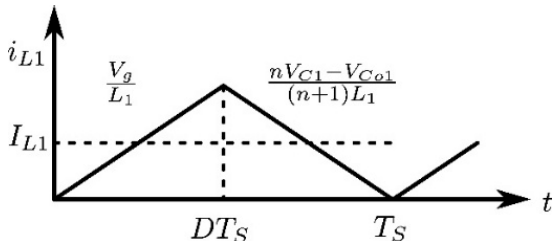

Figure 6. Inductor current $\boldsymbol{L_1}$ $(\boldsymbol{i_{L1}})$ waveform under BCM

The inductor current i_{L1} is shown in Figure 6, Operation in DCM (Figure 5) is achieved when the ripple current Δi_{L1} is greater than the average current, as expressed in (4).

$$I_{L1} = \bar{\imath}_{L1} < \Delta i_{L1} \tag{4}$$

Furthermore, the ripple current Δi_{L1} in the inductor can be calculated using (5).

$$\Delta i_{L1} = \frac{I_{L1,Peak}}{2} = \frac{V_g DT_S}{2L_1} \tag{5}$$

C. Design for Inductors and Capacitors

The sizing of passive components in the converter is critical for maintaining voltage stability and ensuring continuous conduction mode (CCM) operation.

Inductor Design:

To ensure continuous conduction mode (CCM) operation, the inductance must be large enough to prevent the inductor current from reaching zero. The minimum inductance required, denoted as $L_{\text{min,BC}}$, can be estimated using (6).

$$L_{\text{min,BC}} = \frac{V_o\, dd'^2}{4f_s I_o(2n+1+d)} \tag{6}$$

where:

- $L_{\text{min,BC}}$: minimum inductor value for CCM operation,
- V_o : output voltage,
- d: duty cycle (the proportion of T_s during which the switch is on),
- $d' = 1 - d = \frac{T_{off}}{T_s}$: complement of the duty cycle, representing the switch-off duration,
- f_s: switching frequency,
- I_o: output current,

- n: number of D–C–L stages in the converter.

This formulation accounts for energy transfer characteristics during both the switch-on and switch-off periods, and ensures the converter remains in continuous mode.

Capacitor Design:

To limit output voltage ripple within acceptable bounds, the capacitors C_1, C_{O1} , and C_{O2} must be properly sized. The minimum capacitance required for C_1 can be estimated using (7), which is derived under the assumption that the capacitor current can be approximated by its average value during the discharge period, while ensuring charge balance in steady-state operation.

$$C_1 \geq \frac{2V_o}{|\Delta V_{C,\max}| R_L f_S} \quad (7)$$

Where:

- $\Delta V_{C,\max}$: maximum allowable capacitor voltage ripple,
- R_L : load resistance,
- f_s : switching frequency.

This formula is derived by assuming that the capacitor current can be approximated by its average value during the discharge period, and that charge balance must be maintained in steady-state operation.

Output Filter Capacitor:

To smooth out the final output voltage and further reduce ripple, the output filter capacitor C_o must also be selected appropriately. The required minimum capacitance can be calculated using (8).

$$C_o = \frac{dI_o}{\Delta V_{o,\text{maks}} f_S} \quad (8)$$

Where :

- C_o: output filter capacitor,
- d: duty cycle,
- I_o: output current,
- $\Delta V_{o,\max}$: allowable output voltage ripple.

This ensures that the output voltage remains within the desired ripple limits, especially during rapid switching transients.

2.2. Particle Swarm Optimization For Pi Controller

A. PI Controller

The Proportional-Integral (PI) controller is one of the most widely used controllers in industrial applications due to its simplicity and effectiveness. A key aspect of its implementation is the tuning of its parameters to achieve optimal performance. Therefore, a high-speed and accurate tuning method is necessary to determine the control gains Kp and Ki. The control architecture used in this study is illustrated in Figure 7[9], [10].

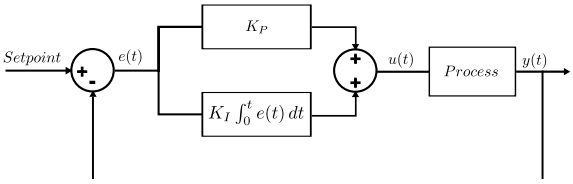

Figure 7. PI Controller System Diagram

The PI control law defines the control signal $u(t)$ as a combination of the instantaneous error and the accumulated error over time. This is mathematically expressed in (9).

$$U(t) = K_p e(t) + K_i \int_0^t e(\tau), d\tau \quad (9)$$

where $e(t)$ is the error signal, and K_p and T_i are the controller gains. The corresponding transfer function of the PI controller is given by (10).

$$G(s) = K_p + \frac{K_i}{s} \quad (10)$$

B. Fundamentals of PSO

Particle Swarm Optimization (PSO) is a heuristic optimization technique inspired by the social behavior of birds and fish. In PSO, a population of potential solutions (called particles) explores the search space by updating their velocities and positions iteratively. Each update is influenced by:

1. The best position previously encountered by the particle itself (p_{best}).
2. The best position found globally by any particle in the swarm (g_{best}).

The velocity of each particle is updated using (11), which combines inertia, cognitive, and social components.

$$v_i^{k+1} = w \cdot v_i^k + c_1 \cdot r_1 \cdot \left(p_{best,i} - x_i^k\right) + c_2 \cdot r_2 \cdot \left(g_{best} - x_i^k\right) \quad (11)$$

Where:

- v_i^k : Velocity of particle i at iteration k.
- w: Inertia weight.
- c_1, c_2 :Cognitive and social coefficients.
- r_1, r_2 : Random numbers [0, 1].
- x_i^k : Position of particle i at iteration k.

Subsequently, the new position of each particle is updated according to (12).

$$x_i^{k+1} = x_i^k + v_i^k + 1 \quad (12)$$

PSO offers a balance between exploration (searching new areas) and exploitation (refining known good solutions), making it effective for solving nonlinear optimization problems[11], [12].

The system diagram for implementing the PSO algorithm in tuning the PI controller is shown in Figure 8. The PI controller is embedded within a closed-loop system where the PSO algorithm adjusts K_p and K_i to optimize system performance based on the feedback error.

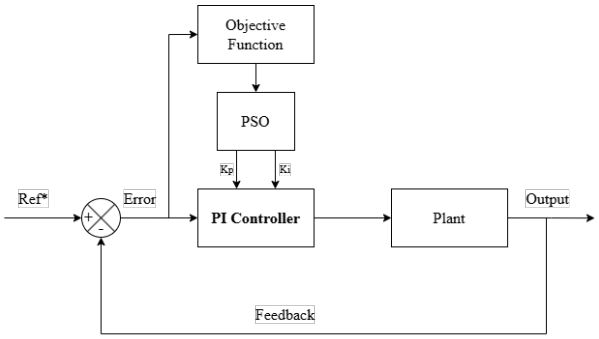

Figure 8. PSO-PI Controller System Diagram

C. Algorithm Design

To systematically implement the PSO algorithm for real-time tuning of the PI controller, a structured procedure is followed. Figure 9 presents the detailed flowchart of this algorithm, highlighting each step from initialization to the identification of optimal control parameters based on system performance feedback.

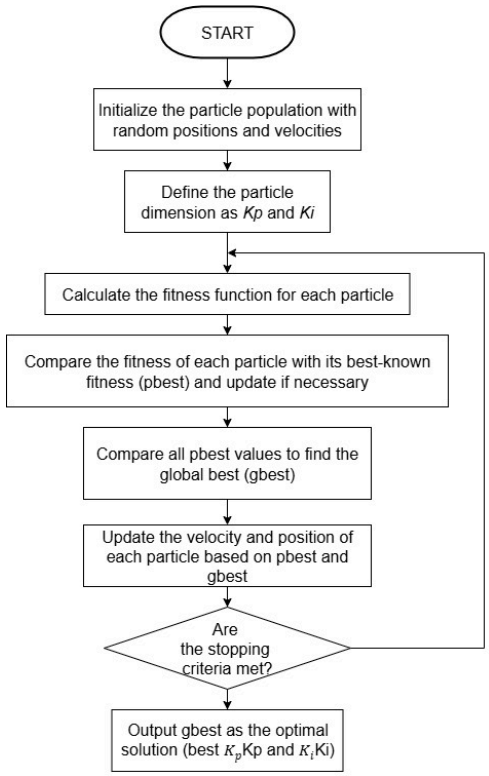

Figure 9. Flowchart of the PSO-PI Controller Algorithm

The PSO-based tuning process is implemented using the following steps:

1. Initialization: Define the number of particles, maximum number of iterations, and PSO parameters (w, c_1, c_2).
2. Fitness Evaluation: Simulate the closed-loop system for each particle and calculate the corresponding fitness value.
3. Velocity and Position Update:
   - Update velocity using the PSO velocity equation.
   - Update position using the new velocity.

4. Convergence Check: Terminate the algorithm when the maximum number of iterations is reached or when the fitness improvement is below a predefined threshold.
5. Output Optimal Parameters: Return the best-performing values of K_p and K_i [13].

3. Results and Simulation

3.1. Simulation Setup

The converter system illustrated in Figure 10 was modeled and simulated in MATLAB/Simulink. The system includes an ultra step-up converter controlled by a PI controller tuned using the Particle Swarm Optimization (PSO) algorithm. The simulation uses a fixed sampling time of $T_s = 0.001\,ms$, and system parameters were chosen to replicate realistic operating conditions. The primary simulation components are summarized in Table 1.

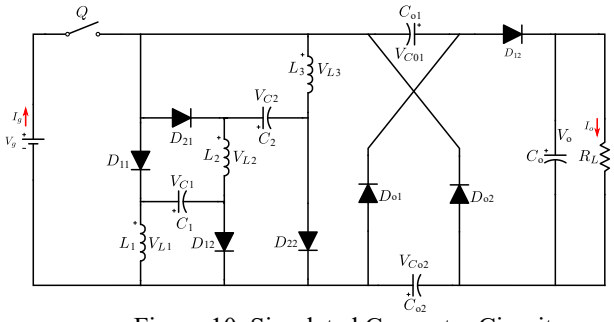

Figure 10. Simulated Converter Circuit

Table 1. Component Values

No.	Parameter	Nilai
1	Input Voltage (Vin)	48 V
2	Output Voltage (Vout)	540 V
3	Output Current (Iout)	1.8518 A
4	Load resistance (R_L)	291 Ω
5	Switching Frequency (f_{sw})	40 kHz
6	Output Voltage Ripple(Δvo)	0.1%
7	Inductor L_1	40.48mH
8	Capacitor C_1, C_{O1}, C_{O2}	192.9 μF
9	Output Filter Capacitor C_{filter}	47μF

To evaluate system performance, load resistance were varied to simulate practical conditions of dynamic loads.

3.2. Open-Loop System

An open-loop simulation was carried out to evaluate the fundamental performance of the ultra step-up converter without any feedback control. In this scenario, the duty cycle was set to 51.02%, as calculated based on the theoretical gain expression. The simulation results show that the converter successfully increased the input voltage significantly, indicating correct operation under open-loop conditions.

The resulting output voltage reached approximately 576 V, slightly higher than the theoretical target of 540 V. This deviation may be attributed to factors such as discrete-time switching control settings, limited resolution in the timing mechanism, or minor numerical effects in the simulation environment. The output voltage profile under this open-loop condition is shown in Figure 11.

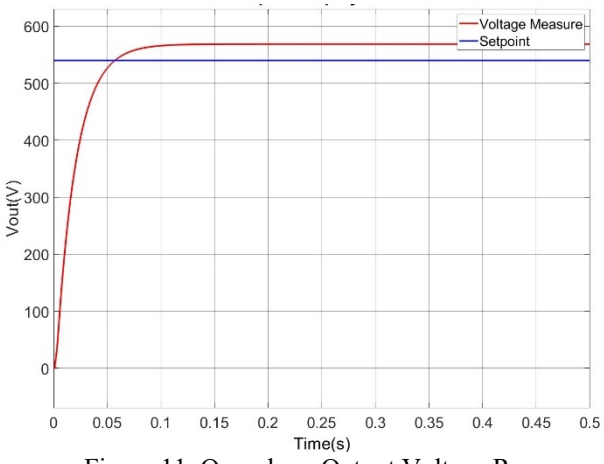

Figure 11. Open-loop Output Voltage Response

3.3. Closed-Loop System Using PSO-Optimized PI Controller vs PI Controller

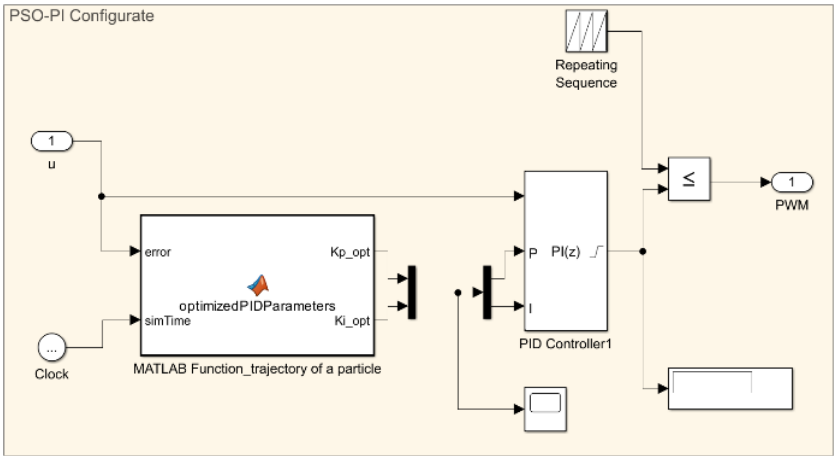

Figure 12. PSO-PI Control

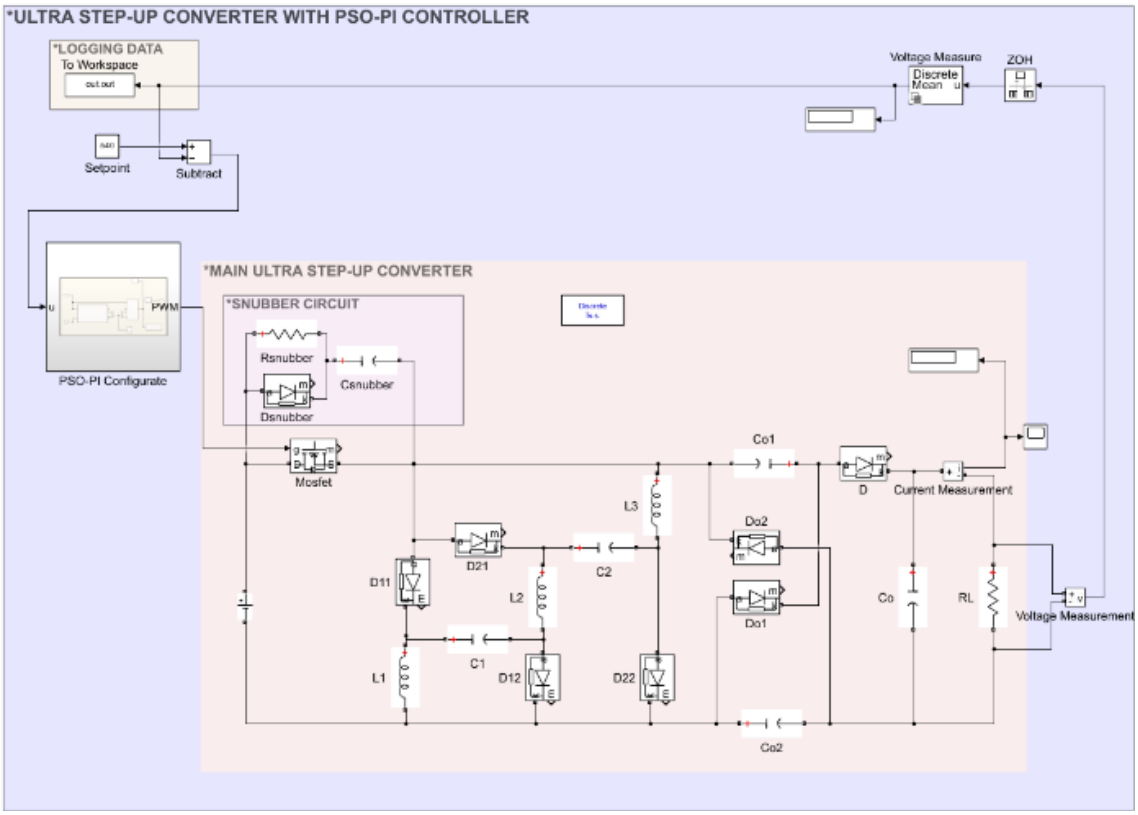

Figure 13. Ultra Step-Up Converter With PSO-PI Controller Simulated

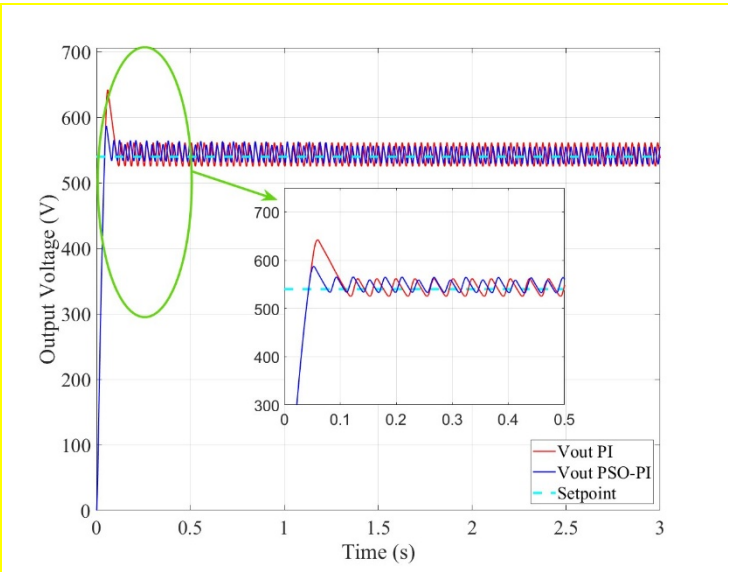

Figure 14. Output voltage response of PI and PSO-PI controller for the setpoint of 540 V

The PSO optimization process was analyzed through particle movement. This analysis illustrates the effectiveness of PSO in identifying optimal PI controller parameters.

PSO implementation parameters:

- Population size: $N = 80$ particles.
- Max iterations: 100.
- Inertia weight (w): w_{max} : 0.9, w_{min} : 0.73
- Cognitive and social coefficients: (c_1, c_2): 2.05.
- Update interval: 0.01 second.

The output voltage response from the PSO-PI system is presented in Figure 18.

As illustrated in Figure 15, the particles were initially distributed randomly across the K_p and K_i parameter space. Over successive iterations, the particles gradually converged toward regions with better fitness values. By iteration 8, the particles had stabilized around the optimal solution, indicating successful convergence of the PSO algorithm.

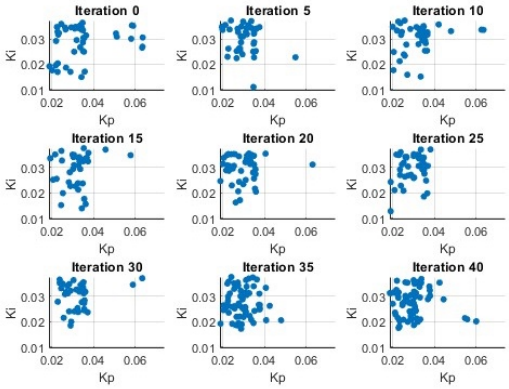

Figure 15. Particle Movement for$\boldsymbol{K_p}$ and $\boldsymbol{K_i}$ Parameters

The PSO-PI controller and PI controller demonstrated enhanced dynamic performance, as detailed in Table 2.

Table 2. Performance Comparison of Open Loop, PI, and PSO-PI Controllers

Controller	Rise Time (t_r) ms	Over shoot (M_p) %	Settling Time (t_s) ms	Steady-State Error (e_{ss})
Open Loop	32.4	0.011	57.4	20
PI	30.1	21.7	227.78	3.464
PSO-PI	31.2	8.7	117.78	9.623

From this comparison, it can be concluded that the PSO-PI controller effectively balances fast response and reduced overshoot, making it more robust and stable for applications involving high voltage regulation. Although the conventional PI controller shows a quicker rise, it suffers from excessive overshoot and prolonged oscillation, potentially impacting system safety and efficiency. Overall, the PSO-based tuning method enhances transient performance and reduces the need for manual gain adjustment, offering a more practical and adaptable control solution.

3.4. Disturbance Test: Conventional PI vs. PSO-PI

To evaluate the robustness of the converter control system, a disturbance test was conducted by introducing step changes in load conditions. The closed-loop system was tested using both a conventional PI controller and a PSO-optimized PI controller.

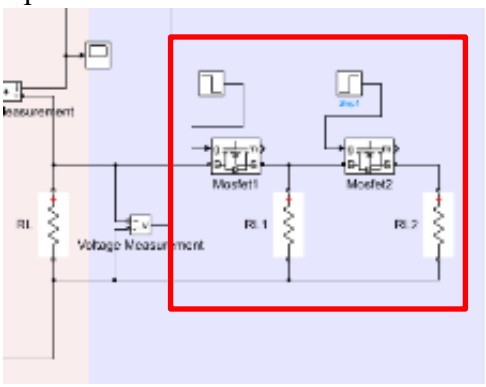

Figure 16. Disturbance Test

As illustrated in Figure 16, the system initially operated under normal conditions with an effective load of 436.5 Ω. At $t = 3\,s$, the load was increased by adding another resistor in parallel, thereby raising the power demand. At $t = 6\,s$, the load was sharply reduced by disconnecting both added resistors. These load transitions were designed to test the controller's ability to maintain voltage stability and suppress oscillations under sudden changes in operating conditions.

A. Output Voltage Performance: Comparison between PSO-PI and Conventional PI Controllers

To evaluate the dynamic performance and robustness of the proposed converter control strategies, a closed-loop disturbance test was performed by applying step changes to the load at specific time intervals. The system response under both the conventional PI controller and the PSO-optimized PI controller was compared based on their ability to maintain output voltage regulation during these changes. The comparison is illustrated in Figure 17, which shows the output voltage behavior over time for both control strategies.

Initially, the system operated under a nominal load condition of approximately 660 W. During this steady-state phase (from 0 to 3 s), both controllers maintained the output voltage close to the reference value of 540 V. However, the PSO-PI controller demonstrated a slightly smoother response with reduced voltage ripple, indicating better steady-state regulation.

At t = 3 s, a load step was introduced by adding an additional resistor in parallel, increasing the total load power to around 1000 W. The conventional PI controller responded with a noticeable voltage drop down to approximately 527 V and exhibited significant oscillations with an amplitude of ±35 V. These oscillations persisted for approximately 0.4 s before the system returned to steady-state conditions. In contrast, the PSO-PI controller experienced a milder voltage dip to around 510 V, but quickly damped the transient within 0.15 s and achieved full stabilization in under 0.7 s.

At t = 6 s, both added resistors were disconnected, resulting in a sharp reduction in load to approximately 330 W. The conventional PI controller once again struggled, showing an overshoot to about 549 V, followed by prolonged oscillations before stabilization. Conversely, the PSO-PI controller showed an overshoot up to 554 V but recovered significantly faster, with complete voltage regulation restored within 0.3 s.

The adaptability of the PSO-PI controller is further demonstrated in Figure 19, which shows the online adjustment of PI controller gains in response to the load disturbances. At each step change, the PSO algorithm updated the values of K_p and K_i dynamically within approximately 0.1 s. For instance, when the load increased at t = 3 s, K_p was reduced and K_i was slightly adjusted to suppress the overshoot and handle the increased demand. When the load decreased at t = 6 s, the gains were adapted in the opposite direction to manage the resulting overshoot. These adjustments played a critical role in achieving fast recovery and minimal voltage deviation, confirming the effectiveness of the PSO-based tuning approach.

In summary, the PSO-PI controller clearly outperforms the conventional PI controller in terms of transient response, overshoot suppression, and recovery time, particularly under large and sudden load variations. This performance advantage is primarily due to its ability to adjust control parameters dynamically and in real time.

B. Load Power Response under PSO-PI and PI Controllers

In addition to voltage regulation, load power behavior was also analyzed to further evaluate the control system's stability and effectiveness during disturbances. Figure 18 illustrates the load power response of the system using both control strategies.

Before the disturbance (t < 3 s), both controllers maintained stable power delivery at approximately 660 W. Upon increasing the load at t = 3 s, both systems responded with a corresponding rise in power. However, the PI controller exhibited significant power ripple and slower convergence to the new steady-state value (~1000 W). In contrast, the PSO-PI controller adapted more effectively, showing faster settling and reduced fluctuation in power delivery.

Following the sudden load reduction at t = 6 s, power dropped sharply to approximately 330 W. The PSO-PI controller again demonstrated superior handling of this transition, stabilizing more quickly with minimal overshoot or undershoot compared to the conventional PI controller.

These results confirm that the PSO-PI controller not only improves voltage regulation but also ensures more stable and efficient power delivery across varying load conditions.

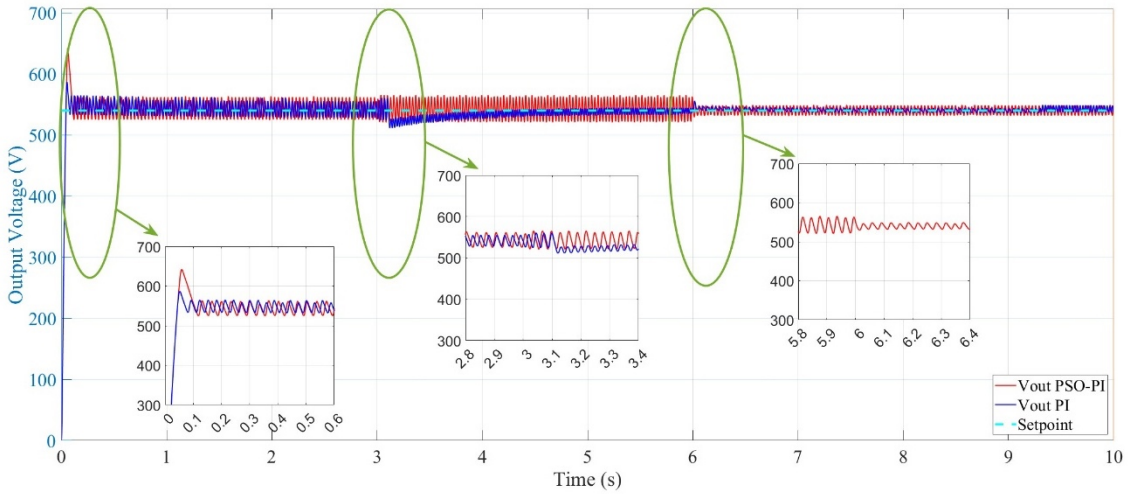

Figure 17. Closed-Loop Output Voltage Response under Load Changes of PSO-PI vs PI Controlllers

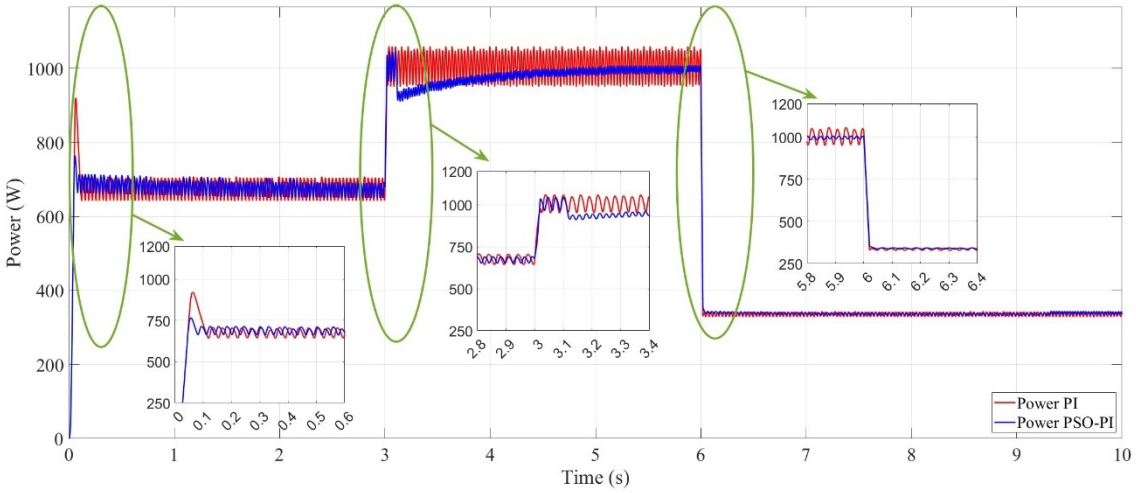

Figure 18. Load Power Changes of PSO-PI vs PI Controlllers

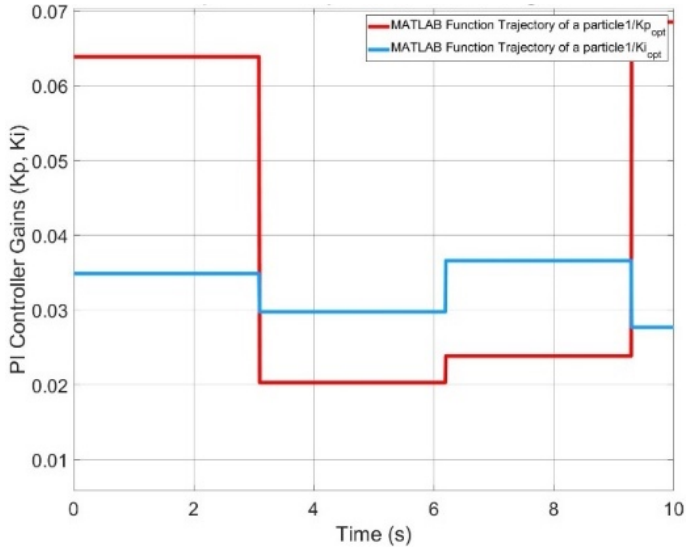

Figure 19. Kp and Ki Response to Power Changes under PSO-PI Control

4. Conclusion

This study demonstrated the effectiveness of integrating a Particle Swarm Optimization (PSO) algorithm into the PI controller design for an ultra step-up DC–DC converter operating under dynamic load conditions. The converter system, designed to elevate a 48 V input into a regulated 540 V output, achieved a gain exceeding 11×. While the open-loop configuration verified basic boosting functionality, it lacked the ability to maintain stability and precision during load variations. Incorporating a conventional PI controller improved voltage regulation, but required fixed, manually-tuned gains. Under disturbance scenarios, the PI controller produced a high overshoot (21.7%), long settling time (227.78 ms), and substantial voltage deviation of up to ±35 V—highlighting its limited adaptability. In contrast, the PSO-PI controller outperformed the conventional approach across all performance metrics. It achieved lower overshoot (8.7%), faster settling time (117.78 ms), and reduced voltage deviation to ±15 V under similar load transients. Moreover, the PSO algorithm dynamically updated K_p and K_i within 0.1 s of disturbance, enabling real-time adaptation to load changes. Recovery times were significantly improved, shrinking from 0.4 s (PI) to as low as 0.15 s (PSO-PI). In terms of load power regulation, the PSO-PI controller exhibited quicker stabilization and

less ripple compared to the conventional PI. Overall, the findings confirm that PSO-based tuning enhances controller robustness, reduces manual configuration effort, and improves both transient and steady-state performance. These advantages make the PSO-PI control strategy particularly suitable for high-gain DC–DC converters in applications with frequent or unpredictable load fluctuations.

5. Recommendations

Considering that this study was conducted entirely through simulation, it is recommended that future research focuses on implementing the PSO-PI controller in a practical hardware setup using platforms such as STM32 microcontrollers. This would allow evaluation of its real-time control performance, computational load, and stability under physical constraints. Further work could also involve integrating the PSO algorithm with other adaptive techniques (e.g., fuzzy logic or neural networks) to enhance responsiveness under rapidly changing load or input conditions. Real-world prototyping and testing—particularly in power electronics systems such as electric vehicle converters or renewable energy interfaces—would be essential to validate the controller's effectiveness beyond theoretical models.

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